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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,242	08/30/2001	Wen Lin	00-LM-117	9379

7590 08/31/2005

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,242	LIN, WEN	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7,10,12 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,10,12 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanenbaum (Operating Systems, Design and Implementation, Prentice-Hall, 1987).

3. With respect to claims 1 and 5, Tanenbaum discloses a computing system (page 114, figure 3-3) comprising:

a processor (CPU) having a data/control bus interface;

a data/control bus (System bus) implementing one or more device communication channels;

a mass storage device (Drive) having an interface for communicating mass storage transactions;

a data memory (Memory) coupled to and shared by both the processor and the mass storage device (see pages 482 – 485, the floppy disk controller driver runs in the Memory and

buffers data for read and write operations, see also page 270, Tanenbaum teaches block or buffer caching of disk blocks); and

a controller (Disk controller with DMA) having a memory interface (interface to the system bus) coupled to the data memory (the controller is coupled to the memory via the system bus) and a mass storage interface (interface to the drive) coupled to the mass storage device's interface (disk controller is coupled to the disk) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device (all disk accesses are conducted through or arbitrated by the controller).

4. With respect to claim 7 the system further comprising storage controller processes (page 92, disk task) and application behavior processes implemented using the processor (page 92, other task, for example, terminal, memory, clock, file system, and user programs).

5. With respect to claim 10, the processor implements data structures storing physical geometry information about the mass storage device (pages 482 – 484).

6. Claims 1 – 3 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunsaker (US Patent Application Pub. No. 2003/0036198).

7. With respect to claim 1, Hunsaker discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a mass storage device (hard drive,176, floppy, 174, and CD ROM 172) having an interface for communicating mass storage transactions; and

a data memory (system memory 140) coupled to and shared by both the processor and the mass storage device (the system memory is shared by the processor via the host bus 120, peripherals via primary bus 195 and other I/O devices including mass storage devices via the ICH 150);

a controller (ICH 150) having a memory interface coupled (150 is coupled to 140 via 130) to the data memory and a mass storage interface coupled to the mass storage device's interface (150 is coupled directly to 170) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

8. With respect to claim 2, the data memory is coupled to the processor by a memory bus (system memory 140 is coupled to the processor via its own memory bus through the controller 130) operating independent of the data/control bus (the host bus 120 and the unlabeled memory bus are independent buses). The Examiner notes that the only configuration where there are two busses directly coupled to the processor is the one shown in figure 6. However this configuration does not meet the controller requirements of claim 1.

9. With respect to claim 3, the controller comprises a memory access controller coupled to the processor, the data memory, and the mass storage device and operable to arbitrate accesses to the data memory between the mass storage and the processor (the controller MHC 130 controls access to the system memory and is the nexus that connects all of the claimed elements).

10. With respect to claim 21, the mass storage device comprises an optical storage device (CD ROM 172).

11. Claims 1, 12, 13 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaidi *et al.* (US Patent No. 6,601,126, hereinafter "Zaidi").

12. With respect to claim 1, Zaidi discloses a computing system (figure 28) comprising:

a processor having a data/control bus interface(CPU);

a data/control bus (CPU bus) implementing one or more device communication channels;

a mass storage device (DMA peripheral, see col. 27, lines 41 – 45) having an interface for communicating mass storage transactions; and

a data memory (DRAM) coupled to and shared by both the processor and the mass storage device (neither the CPU nor the DMA peripherals have exclusive access to the DRAM memory, the DRAM is shared by all components that has access to it);

a controller (bridge and MAC) having a memory interface coupled to the data memory (MAC is coupled to DRAM) and a mass storage interface coupled to the mass storage device's interface (bridge is coupled o DMA peripherals) and operable to conduct mass storage

transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

13. With respect to claim 12, (figure 1, and col. 4, lines 27 – 46, figure 28 is one of the embodiments of this system on chip) the controller is integrated with the processor on a single integrated circuit chip.

14. With respect to claim 13, the mass storage device's interface comprises a peripheral component interconnect (PCI) standard-compliant interface (figure 28).

15. With respect to claim 20, the computing device comprises a network appliance (col. 27, lines 40 – 45, in a networking application one of the DMA peripherals would be a network controller) having a network controller coupled to the data/control bus.

16. Claims 1, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty *et al.* (US Patent No. 6,128,669, hereinafter "Moriarty").

17. With respect to claims 1 and 14, Moriarty discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (100);

a data/control bus (102) implementing one or more device communication channels;

a mass storage device (144) having an interface for communicating mass storage transactions;

a data memory (104, or alternatively 112) coupled to and shared by the processor and the mass storage device; and

a controller (106, or alternatively 106 and 108) having a memory interface coupled to the data memory (106 is coupled to 104) and a mass storage interface coupled to the mass storage device's interface (106 is coupled to 120) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

18. With respect to claim 20, computing device comprises a network appliance having a network controller coupled to the data/control bus (network controller 128 is coupled to 102 through 106).

19. Claims 1, 13 – 16, and 20 – 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Yiu *et al.* (US Patent Application Pub. No. 2003/0181205, hereinafter "Yiu").

Yiu discloses a computing system (figure 3) comprising:

a processor having a data/control bus interface(31);

a data/control bus (41) implementing one or more device communication channels;

a mass storage device (34) having an interface for communicating mass storage transactions;

a data memory (33) coupled to and shared by the processor and the mass storage device (shared via the bus 41); and

a controller (page 3, paragraph 34) having a memory interface coupled directly to the data memory and a mass storage interface coupled directly to the mass storage device's interface (all of the devices in figure 3 are coupled directly through the system bus 41) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

Yiu discloses various interfaces claimed in claims 13 – 16 (page 3, paragraph 34), and mass storage types claimed in claims 21 – 22 (page 3, paragraph 35). A network controller of claim 20 is disclose as well (figure 3,37 – 38, page 3, paragraph 36)

20. Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellison *et al.* (US Patent Application Pub. No. 2002/0144121, hereinafter "Ellison").

Ellison discloses a computing system (figure 1C) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a mass storage device (hard drive,176, floppy, 174, and CD ROM 172) having an interface for communicating mass storage transactions;

a data memory (system memory 140) coupled to and shared by the processor and the mass storage device; and

a controller (ICH 150) having a memory interface coupled to the data memory (150 is coupled to 140 via 130) and a mass storage interface coupled to the mass storage device's interface (150 is coupled to 170) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

The computing system comprises a set-top box including processes for implementing audio/video behaviors in the processor (page 1, paragraph 13).

21. Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Houston *et al.* (US Patent No. 6,493,656, hereinafter "Houston").

Houston discloses a computing system (figure 1) comprising:

a processor (100) having a data/control bus interface;

a data/control bus (104) implementing one or more device communication channels;

a mass storage device (118, 122) having an interface for communicating mass storage transactions;

a data memory (106) coupled to and shared by the processor and the mass storage device; and

a controller (102, or 102 and 114, or 102 and 121) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and

operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands (col. 1, lines 37 – 52);

a servo controller coupled the data memory by the controller and configured to generate the commands to the actuator mechanism (figure 2).

22. With respect to claim 18, the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism (col. 5, lines 27 – 37).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
August 25, 2005